The Road to Gate-All-Around CMOS

IEEE Solid-State Circuits Society
IC Innovation

Alvin Loke

IEEE Solid-State Circuits Society
Distinguished Lecture

Contact
Intel, San Diego
alvin.loke@alumni.stanford.edu

Bio

Alvin Loke is a Senior Principal Engineer at Intel in San Diego, working on analog design and technology co-optimization for gate-all-around CMOS technologies. He has contributed to CMOS nodes from 250 nm to 2 nm at Agilent, AMD, Qualcomm, TSMC, and NXP, and holds a BASc from the University of British Columbia and MS and PhD degrees from Stanford. His work focuses on analog and mixed-signal design, particularly wireline links, chiplet I/O, and design–technology interface methodologies. He is an active IEEE Solid-State Circuits Society leader and Distinguished Lecturer who frequently presents short courses and invited talks at major conferences such as ISSCC, VLSI Symposium, and CICC.

Event Information:

Date: **May 1**
Time: **10:00 AM – 11:15 AM** (Pacific Time)
Location: **Virtual** (**Zoom**)
Zoom Meeting Link:
https://csus.zoom.us/j/82673642286
Meeting ID: 826 7364 2286

Abstract:

Despite the much-debated end of Moore's Law, CMOS scaling still maintains economic relevance with 2nm gate-all-around SoCs (Intel 18A) already in high-volume manufacturing since January 2026. Area scaling extensively driven by design/technology innovations co-optimized for primarily logic scaling continues to offer compelling node-to-node power, performance, area, and cost benefits.

In this tutorial, we will start with a walk through memory lane, recounting a brief history of transistor evolution to motivate the migration from the planar MOSFET to the fully depleted FinFET. We will summarize the key process technology elements that have enabled the finFET CMOS nodes, highlighting the resulting technology characteristics and challenges. This will set the stage for transitioning to the nanoribbon gate-all-around device architecture and unveiling the magic of how these devices are fabricated.