

Upcoming CXR MPW Shuttle

Next CXR CMOS+X Shuttle (Advanced Node)

CXR is preparing its next full-reticle CMOS+X MPW shuttle leveraging TSMC 28nm technology, enabling advanced post-CMOS innovation for AI, quantum, sensing, and emerging hardware applications.

Important Dates

- March 17, 2026 - CXR Information Session (Town Hall) - Program details, technology flavor, participation model, and Q&A
- March 25, 2026 - CXR Shuttle applications open
- April 15, 2026 - User selection in process
- November 10, 2026 - Target tapeout date

Technology

Foundry: TSMC

Node: 28nm CMOS

Act Early

Participation is limited, and shuttle seats are allocated on a competitive basis. Early engagement is strongly encouraged to ensure alignment with design, fabrication, and +X integration requirements.

**Reserve your place in our next CXR MPW shuttle!
Capacity is limited.**

For participation and partnership inquiries:

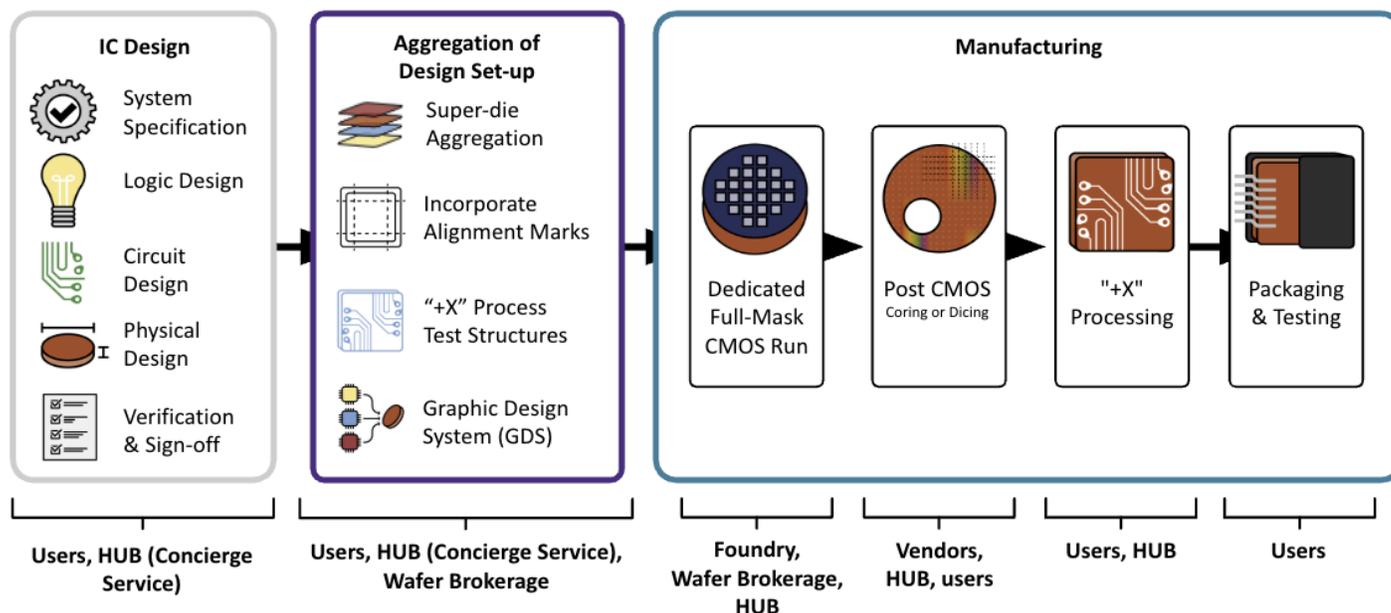
pacific-nw-ai-hub@stanford.edu



Objective: To establish **CMOS+X route (CXR)** for the Microelectronics Commons to accelerate lab-to-fab for transition; “X”: RF/MS, FeFET, FeRAM, CNFET, RRAM/MRAM, gain cell memory, NEMS/MEMS, photonics, etc. The pilot for the end-to-end demo run aims to stand up the CXR infrastructure (including vendors) and concierge service to CXR Users.

Background: CMOS+X using standard CMOS from foundries enables “+X” processing at the metal level for a wide range of applications. The CMOS+X route provides Users a clear path to implement user-specific CMOS+X with shared cost CMOS run, along with enabling technical support from the California-Pacific-Northwest AI Hardware Hub ([NW-AI Hub](#)).

CXR Journey:



CXR Pilot Cost: The principle of “at cost”; For this pilot the Hub will **cover** the cost of CMOS foundry run and standing up key infrastructure including (a) post CMOS processing at the Hub and (b) concierge service in design & integration, both provided to Users at cost. The “+X” technology integration cost and design cost will be self-supported by individual Users.

Pilot Coordination: Provided by NW-AI Hub, including teaming of the Users, aggregation of User designs, securing CMOS run through a wafer brokerage, conducting foundry CMOS run and post-CMOS processing to enable “+X” processing, which would then be coordinated by the User. NW-AI Hub may perform the “+X” processing for Users (for additional cost) when the technology requested is available.

CMOS & Post-CMOS: Dedicated tapeout with 300 mm 40 nm CMOS, yielding full wafers for subsequent processing (participants may order the numbers of wafers they need at cost, subject to project requirements). Post-CMOS processing to produce whole wafers (e.g. 100 – 200 mm) or coupons (e.g. >1 cm x 1 cm) per User’s specification, including any necessary cutting, back-grinding and beveling and pad opening (supported by the Hub at cost), and User funded “+X” processing, packaging and testing.

CXR timeline (targeted): Soliciting & teaming of Users (up to 20) – 2 months; User design, aggregation & CMOS run setup – 5 months; CMOS run & post-CMOS – 3 months.

Concierge Service: Hub to provide general design and process integration support to Users; Hub to provide post-CMOS processing support to enable subsequent “+X” processing by the User’s choosing.

Contact Portal: To receive more information about becoming a **User** or a **vendor**, please contact: **Kia Omid-Zohoor** pacific-nw-ai-hub@stanford.



Unlocking the Future of AI Hardware with CXR: Democratizing CMOS+X Innovation

The integration of commercial-grade semiconductor CMOS technologies with emerging "X" technologies—such as 2D materials, quantum components, and functional materials—represents a transformative leap beyond traditional device scaling. This convergence not only overcomes the limitations of conventional semiconductor approaches but also accelerates the path to commercialization. However, innovators face significant barriers in accessing the necessary infrastructure: high design and mask costs for foundry runs, intellectual property (IP) concerns in multi-project wafer (MPW) services, and a lack of post-processing expertise for integrating "X" technologies. These challenges restrict the adoption of CMOS+X solutions to only a select few, stifling broader innovation.

To bridge this gap, the **NW-AI Hub** introduces **CXR (CMOS +X Route)**, a pioneering initiative designed to democratize access to **CMOS+X technologies** for AI hardware implementation. By leveraging **commercial-grade fabrication resources** and **specialized technical expertise**, CXR empowers innovators, startups, and industry partners to rapidly prototype and scale next-generation semiconductor solutions.

Why CMOS+X? A Faster Path from Research to Commercialization

Unlike approaches requiring fundamental CMOS-level retooling, CMOS+X builds on existing industry infrastructure, dramatically shortening the timeline from concept to market-ready technology. This makes it an attractive strategy for researchers, funding agencies, and commercial partners seeking near-term impact.

Key Benefits of CXR:

- 1. Streamlined Access to Advanced Fabrication**
 - Aggregates multiple research projects into **cost-effective Multi-Project Wafer (MPW) runs**, eliminating the prohibitive costs of standalone foundry access.
 - Ensures **IP protection and confidentiality**, addressing a critical limitation of traditional commercial MPW services.
- 2. End-to-End Post-Processing Expertise**
 - Provides seamless integration of "X" technologies through partnerships with leading facilities, including **Berkeley Marvell Nanolab, Stanford Nanofabrication Facility (SNF), UC Davis Center for Nano-MicroManufacturing (CNM2), and Western Digital's Nanoscale Lab.**
 - Enables rapid prototyping, testing, and optimization of hybrid CMOS+X devices.

Driving the Next Wave of AI Hardware Innovation

CXR removes the traditional barriers to CMOS+X adoption, fostering a collaborative ecosystem where researchers and industry can accelerate breakthroughs in AI, quantum computing, and beyond. By providing **scalable, cost-efficient, and secure access** to cutting-edge semiconductor technologies, CXR ensures that the next generation of hardware innovation is not limited to a few—but accessible to all.

For additional details and future updates regarding the next CXR shuttle, please visit our website. A CXR Information Session for the second shuttle will be held on March 17, 2026.

Join the CMOS+X advantage. Scale faster. Innovate without limits.

(For partnership and participation inquiries, contact pacific-nw-ai-hub@stanford.edu)

