Bridging Institutions Through Semiconductor Research
November 2025 | Grace Hsieh

Undergraduate visiting researcher Andrea Murillo Martínez reflects on a transformative summer internship at Stanford University in the Nanoelectronics & Nanotechnology Lab, part of the California Pacific Northwest AI Hardware Hub initiative.

“There’s always more to learn. You never really stop.”

This past summer, from June to August, Andrea Murillo Martinez, an undergraduate Electrical Engineering student from the University of Hawai‘i at Mānoa, was on a journey that took her from the islands to the heart of Silicon Valley. As an Undergraduate Visiting Research Intern at Stanford University, Andrea worked on a cutting-edge chip design project that not only pushed the boundaries of microelectronics but also helped clarify her path forward: toward a Ph.D. and a future in advanced research.

From Curiosity to Circuitry
Originally from Mexico, Andrea came to UH Mānoa as an international student with a passion for engineering and problem-solving. Now in her senior year, she’s pursuing the Electrophysics track in the Department of Electrical Engineering.

“I always knew I wanted to go into engineering,” Andrea says. “I tried a bit of everything – mechanical systems, embedded systems – but eventually realized I wanted to go deeper. I wanted to understand what was really happening at the transistor level.”

That curiosity led her to pursue research opportunities outside the classroom. Thanks to mentorship from Professor Boris Murmann, a former Stanford professor now based at UH Mānoa, Andrea was introduced to Professor H.-S. Philip Wong at Stanford, who welcomed her into his research group for the summer.

Building Smarter Memory from the Ground Up
At Stanford, Andrea joined a team focused on designing a next-generation image buffer using oxide semiconductor gain cells, a smaller and more energy-efficient alternative to traditional SRAM memory. The goal: to explore new ways of building memory systems that are both compact and high-performing.

The work is part of a larger chip integration effort involving multiple design blocks and contributors. Weekly team meetings and ongoing cross-functional collaboration ensure that all components come together seamlessly.

“This isn’t just a theoretical project,” Andrea explains. “We’re preparing for a real tape-out. That means we’re designing, simulating, and laying out the chip – all the way to manufacturing.” Andrea worked on multiple phases of the chip design process, starting with chip integration on the pin I/O, followed by digital block simulations, and later focusing on the analog domain, where she was involved in the design of the readout circuitry. Across these stages, she has used Cadence tools for schematic design, circuit simulation, and validation. She collaborates closely with graduate students Xinxin Wang and Yiming Tan and has quickly adapted to the lab’s fast-paced, hands-on nature of the work.

Learning by Doing (and Debugging!)
Despite being a newcomer to Stanford’s lab culture, Andrea quickly moved beyond initial learning curves, developing the insight needed to understand circuit operation and refine designs effectively.

“At first, I didn’t know what to expect,” she says. “But running into errors turned out to be the most valuable part. It taught me how to ask the right questions, use the tools effectively, and really understand the fundamentals.”

She also discovered just how much of chip design relies on simulation, a detail that initially caught her off guard. “You have to simulate everything, from schematic-level operation and mismatch variations using Monte Carlo to post-layout verification, to ensure each block functions as intended when manufactured. This is especially true in analog design, where even minor variations can lead to unexpected behavior.”

Through it all, Andrea says collaboration and mentorship have made the experience deeply rewarding. “You learn so much just by working alongside others. This isn’t the kind of work you do alone.”

A Broader Perspective
Beyond the lab, Andrea immersed herself in Stanford’s interdisciplinary research culture by attending talks, dissertation defenses, and events that gave her exposure to a range of topics and technologies.

“It’s been humbling and inspiring,” she says. “At UH Mānoa, the research groups are smaller, which means you get to know everyone and work closely with your mentors. Here, it’s a different kind of energy. There is so much happening at once, with teams tackling projects across many areas of research.”

Andrea’s curiosity about how research unfolds across campuses began before her work with Stanford. While attending the 2024 NAESC West Regional Conference at Oregon State University, she had the opportunity to tour a fabrication lab, gaining early insight into the variety of approaches that universities take in AI hardware research. The experience gave her a

firsthand perspective on how different campuses organize hands-on research and technology development, perspectives that echo the California Northwest AI Hardware Hub's mission of fostering cross-campus collaboration and innovation.

Looking Ahead
As Andrea continues with her final year at UH Mānoa, she does so with a sharper focus and greater confidence in her path ahead.

"This summer confirmed it – I want to do a Ph.D.," she says. "I've always been interested in research, but now I know I want to keep going. There's so much more to learn."

When asked to sum up her experience in one word, she didn't hesitate to say: "Transformative." "It completely changed the way I think about research. It's independent. It's problem-solving. And it's never-ending – in the best way."

About the Internship
Andrea Murillo Martínez participated as a Visiting Undergraduate Research Intern at Stanford University, where she gained exposure to the Northwest AI Hardware Hub, a cross-institutional initiative advancing next-generation semiconductor technologies and collaborative research. The Hub unites more than 60 academic, national lab, and industry partners, including Stanford University, the University of Hawai'i at Mānoa, Oregon State University, and others, working together to accelerate the lab-to-fab transition of AI hardware innovations. Although her internship was not an official Hub partnership, it reflects the kind of cross-institutional collaboration the Hub seeks to foster.