CXR Service Center & 28nm MPW Shuttle

Enabling Advanced-Node Silicon for +X Innovation

Philip Wong
Mar 17, 2026

Meeting Agenda

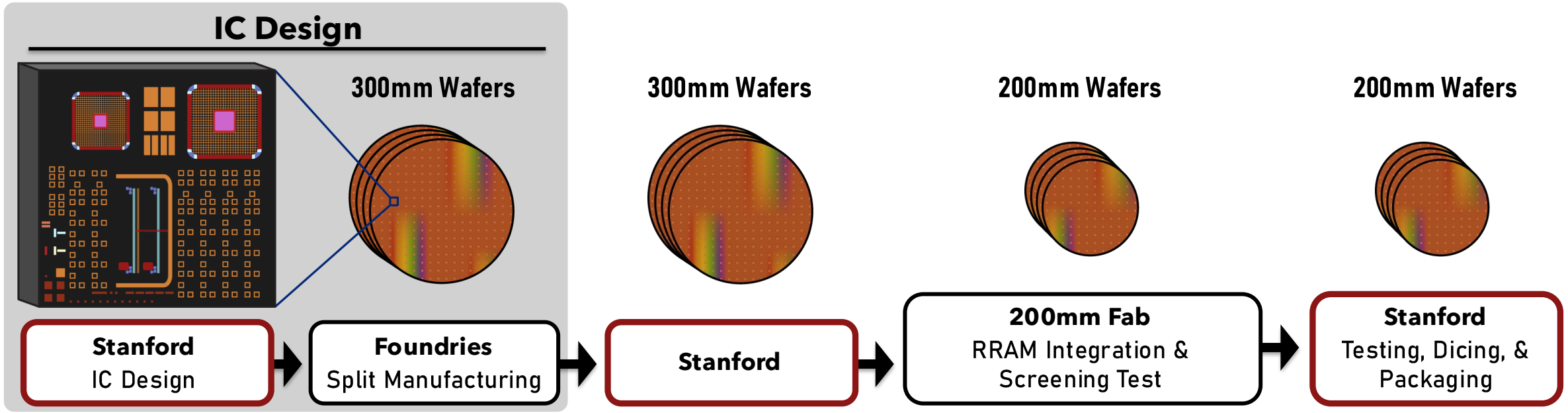
- CMOS+X Route
- CXR Service Center
- Open Q/A – all

CMOS + X

Advanced nodes, new applications, new markets, broad societal impacts

- **CMOS logic + memory**
- **CMOS logic + photonics**
- **CMOS logic + spintronics**
- **CMOS logic + power electronics (GaN, SiC…)**
- **CMOS logic + nanomechanics**
- **CMOS logic + sensors/actuators (brain interfaces, retinas…)**
- **CMOS logic + RF/mm-wave (5G, 6G…)**
- **CMOS logic + quantum computing (control circuitry)**
- **…**

CMOS+X Example with Wafer Coring



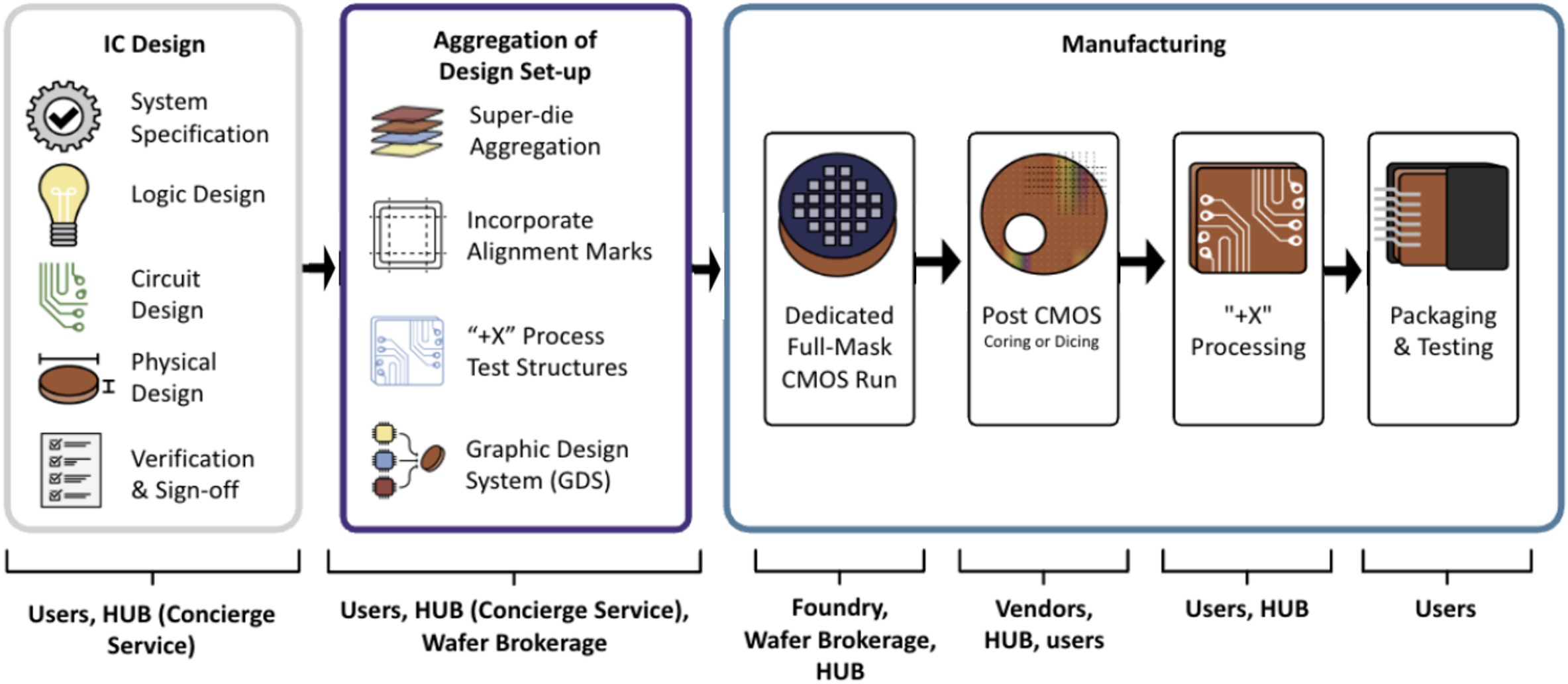
Example of Past Success: >90% yield at the memory macro level achieved

"Resistive switching random access memory – device scaling in 3D architecture and integration with complementary metal oxide semiconductor", Joon Sohn, Ph.D. dissertation (2018)

J. Provine…S. Mitra, H.-S. P. Wong, S. Wong, "Advances in RRAM Through Split Manufacturing and Aggressive Scaling," GOMAC paper 7.1 (2014).

Cored wafers for advanced prototyping at "+X" facilities and foundries!

The Journey CXR (CMOS+X Route)



*Enabling **Coordination** and **Support** to External Users for CMOS+X Prototyping*

California-Pacific-Northwest AI Hardware Hub

CXR Service Center

Kia Omid-Zohoor

Mar 17, 2026

CXR Service Center

Core Services Offered

- **Access to advanced CMOS foundry technologies**
- **Design enablement (e.g., PDKs, technology/design interface protocols)**
- **NDA management and secure IP handling**
- **CXR operates as a concierge service, offering hands-on technical guidance to support users across the full flow, including:**
  - Technology integration and design enablement
  - Coordination of **wafer preparation services (couponing, coring, dicing, thinning, etc.)**
  - Connection to **qualified and audited Si-processing vendors** familiar with advanced-node handling

- **Unlike traditional MPW brokers, CXR provides access to full wafers (not ablated), allowing users to perform post-processing and +X integration on top of advanced CMOS platforms — making heterogeneous and emerging technology integration feasible**
- **The service is designed for early-stage, high-risk, and disruptive projects, including dual-use, academic, startup, and national-lab efforts, where customization, IP protection, and post-processing flexibility are critical.**

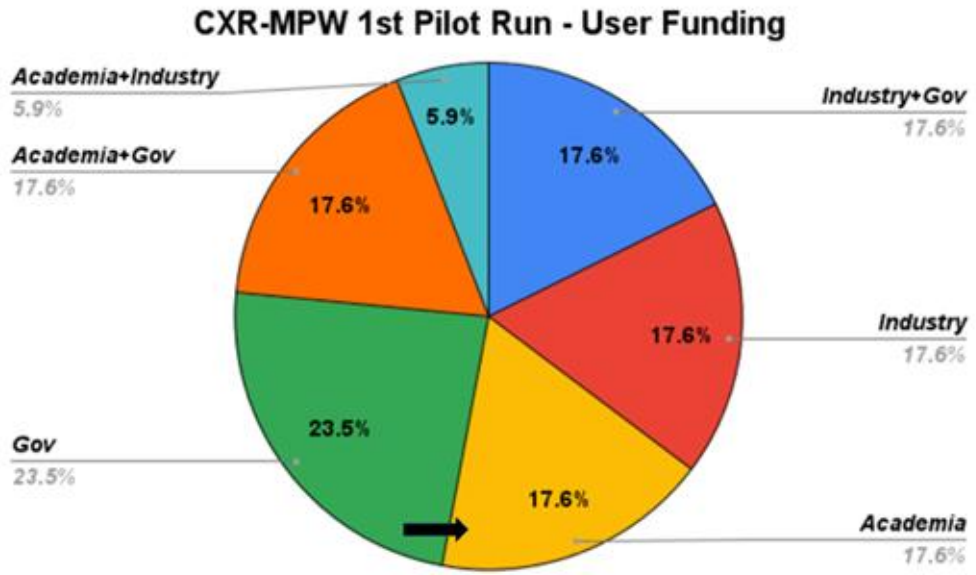
CXR Service Center

Early Milestones & Successes:

- MPW pilot projects started from startups, universities and national lab
- Partnership with TSMC for fabrication of initial projects
- Executed a multi-party NDA with TSMC in record time for secure, streamlined access to their process
- First CXR MPW shuttle taped out in Jan 2026 (fab-out expected May 2026)
- Multiple Hub members have already requested seat reservation for the next CXR MPW shuttle (2026)

CXR 40nm Pilot

- **Sixteen projects from Academia, industry, academia & industry (JV) and national lab have participated in CXR first MPW shuttle**



Upcoming CXR Shuttle Technology – TSMC 28nm

- Proven **28nm planar CMOS technology** widely used in industry and academia
- Optimized for **High Performance Computing, AI, Networking, and Advanced SoC research**
- Mature node → high yield, stable models, strong ecosystem
- Ideal for: **AI / ML accelerators, Custom processors, Mixed-signal SoCs, Photonics / sensors / University & startup prototypes**

Technology features (high-level):

- 28nm planar CMOS logic
- Multi-Vt transistor options (HVT / SVT / LVT/ ULVT)
- Multiple metal stack options (high-density / thick-metal variants)
- Standard cell libraries available
- Memory compiler support (SRAM)
- Wide I/O support (low-voltage & high-voltage options)
- GPIO / high-speed I/O / SerDes-class research (if available via libraries)
- Compatible with industry-standard EDA flows

Next Shuttle & How to Join

Next Steps for Joining the CXR 28nm Shuttle

Important Dates:

- March 17, 2026 — CXR Information Session (Town Hall)
- March 25, 2026 — Shuttle Applications Open
- April 15, 2026 — Selection in-process
- November 10, 2026 — Target Tape-Out Date

How to Apply

- Application form will be available on the **NW-AI Hub / CXR website**
- Link will be sent to all townhall attendees
- Participation requires **Hub membership (limited NDA) –** **Membership is not required for shuttle application**

CXR Shuttle Model

- Private MPW shuttle
- Secure multi-party NDA framework
- Full wafers available for +X / post-processing integration
- Concierge support throughout the flow. Participant MUST have a clear +X implementation plan

Thank You
Northwest AI Hub site for more info:

nw-ai-hub.org

Open Q/A

What is the cost to participate?

- **NW-AI Hub funds the full mask set (> $1.1M)**
- **Users pay only for:**
  - Wafers they request (~$8.5K–$9.5K per wafer, estimate)
  - Optional services:
    - wafer coring / couponing / thinning
    - +X processing
    - packaging
    - engineering support

Cost varies depending on:

- number of wafers
- +X complexity
- packaging / test needs

Can startups participate?

- Yes — CXR is designed for:

  startups, industry R&D teams, universities & national labs

Selection Process & Participation Criteria

What are the selection criteria for the CXR MPW shuttle?

User Expectations

- Project must be compatible with the selected standard CMOS foundry process (TSMC 28nm) with post-CMOS integration at the top metal / BEOL level (+X)
- Users retain full IP ownership, but must acknowledge that their design will be fabricated on a shared MPW reticle with other participants
- All participants must be Microelectronics Commons Hub members
- Each User must define a clear plan for post-CMOS (+X) processing, funded by the User
- Export / Handling Restriction: All CXR-fabricated silicon (including wafers, diced chips, and coupons) must remain within the United States. Distribution, shipment, or transfer outside the U.S. is not permitted
- Participants must be US entities.
- Users are expected to provide a brief technical outcome summary within ~6 months after wafer delivery

Selection Process & Participation Criteria

Selection Process

- Target cohort: ~20–25 projects per shuttle
- Each proposal reviewed by CXR team for technical fit, readiness, and compatibility
- Final approval by NW-AI Hub leadership / Executive Committee
- Priority given to projects aligned with:
  - AI hardware / microelectronics innovation
  - CMOS+X integration is a MUST
  - National security / innovation/ commercialization relevance
  - Technical readiness for the tapeout schedule

Are there required agreements?

For the upcoming shuttle, the following agreements will be required for selected participants:

- **Hub Membership Agreement –** All CXR shuttle participants must be members of NW-AI Hub. This is required to ensure proper IP protection, program compliance, and eligibility for participation.
- **Multi-party NDA (4-way NDA) –** A confidentiality agreement will be executed between the User, CXR / NW-AI Hub, the wafer broker, and TSMC to enable secure access to the PDK, design information, and foundry services.
- **CXR User Participation Agreement –** This agreement defines the scope of participation, including user responsibilities for wafer costs and any optional downstream services such as wafer coring, dicing, couponing, thinning, or +X processing, if applicable.

Do we need our own TSMC agreement?

- No. Access to TSMC is coordinated through CXR.

What Happens After the Townhall? (Next Steps)

What should applicants do next?

User Responsibilities

- **Submit application questionnaire (after March 25)**
- **Provide:**
  - CMOS design requirements (area, device type, metal stack, etc.)
  - Detailed **+X / post-CMOS plan**
  - Substrate / wafer / coupon needs
  - Testing / packaging plan (if known)
- **Confirm Hub membership**
- **Review and sign required agreements**

CXR / Hub Responsibilities

- Review technical compatibility of each project & User Selection
- Coordinate NDA / membership / participation agreements
- Manage foundry interface and shuttle logistics (tapeout, verification, etc)
- Coordinate wafer handling, dicing, couponing, +X support

Where can +X processing be done

- Users fund their own +X processing, packaging, and testing
- +X can be performed at:
  - NW-AI Hub facilities (SNF, BANano, partner labs)
  - Other Commons Hubs (CA DREAMS, SWAP, SCMC, MMEC, etc.)
  - Industry partners (when applicable)

- CXR can provide:
  - Process integration guidance
  - Vendor coordination
  - Post-CMOS substrate preparation
  - Engineering support

What is the die size limit?

- Depends on total reticle allocation
- Typical MPW blocks: few 1x1 mm^2 to ~4x4 mm^2 range
- Final allocation depends on number of users

What technology options are available?

Current shuttle:

- TSMC 28nm CMOS (The specific version of 28nm will be determined based on CXR Users' need)
- Standard metal stack
- Post-CMOS +X integration allowed

Future runs may include:

- **other nodes**
- **multiple shuttles per year**

Is this a private shuttle?

- Yes.
- Only CXR-approved users participate
- Not a public MPW
- Additional IP protection through NDA